Hindawi Publishing Corporation
Journal of Nanotechnology
Volume 2011, Article ID 823680, 4 pages
doi:10.1155/2011/823680

*Research Article*

# All-Printed Thin-Film Transistor Based on Purified Single-Walled Carbon Nanotubes with Linear Response

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Received 29 April 2011; Revised 1 July 2011; Accepted 7 July 2011

Academic Editor: Yoke Khin Yap



We report an all-printed thin-film transistor (TFT) on a polyimide substrate with linear transconductance response. The TFT is based on our purified single-walled carbon nanotube (SWCNT) solution that is primarily consists of semiconducting carbon nanotubes (CNTs) with low metal impurities. The all-printed TFT exhibits a high ON/OFF ratio of around $10^3$ and bias-independent transconductance over a certain gate bias range. Such bias-independent transconductance property is different from that of conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) due to the special band structure and the one-dimensional (1D) quantum confined density of state (DOS) of CNTs. The bias-independent transconductance promises modulation linearity for analog electronics.

## 1. Introduction

Printable flexible electronics technology offers a cost-effective way to achieve mass production of large-area flexible electronic circuits without using special lithography equipment. It is expected to offer an enabling technology for numerous applications, particularly those that require or may benefit from the use of flexible polymeric substrates, such as inflatable antennas, electronic papers, RF identification (RFID) tags, smart skins, and flat panel displays. Due to its mechanical flexibility and high field effect mobility, carbon nanotube (CNT) has shown great promises in printable flexible electronics [1–5]. High mobility and high-speed CNT-based printable thin-film transistor (TFT) have been demonstrated [6–10]. In addition to its mechanical flexibility and high field effect mobility, CNT is also a promising material for transistors with bias-independent transconductance due to the special band structure and the one-dimensional (1D) quantum confined density of state (DOS) of CNTs [11–14]. The band structure and the 1D DOS of CNT allow the CNT-based TFTs to possess near-ballistic electron transportation and bias-independent transconductance [12, 13]. Such bias-independent transconductance is called inherent linearity [12] (referred it to as linear response or linear CNT-TFT, henceforth). The bias-independent transconductance is different from conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) and is highly desired in many analog RF devices such as low noise amplifiers and power amplifiers [11–13]. However, most linear CNT-TFTs reported to date are based on CNTs grown by using the

chemical vapor deposition (CVD) grown method [12, 13] to obtain semiconducting CNTs with good alignment between the source (S) and drain (D) electrodes [13]. While high density aligned CNTs can achieve the highest performance [13], however, due to the high CVD-growth temperature of over 900°C, the CVD grown CNTs are not suitable for the development of printed flexible electronic devices [9]. Purified CNT solutions allow one to print CNT networks on flexible substrates with high field-effect electron mobility [9] and high-speed performance [10] for above-mentioned low-cost printed flexible electronics applications. In this paper, we evaluate the linear response of a CNT-TFT printed at room temperature using our purified single-walled carbon nanotube (SWCNT) solution consisting primarily of semiconducting carbon nanotubes (CNTs) with low metal impurities. The all-printed TFT shows a high ON/OFF ratio of around $10^3$ and bias-independent transconductance over a certain gate bias range. Subthreshold swings of the all-printed TFT are also analyzed and agree well with the CVD-grown CNT-TFTs [12, 13]. The linear response shows that the printed CNT-TFT is promising for analog electronics that requires modulation linearity.

## 2. Experiment

The all-printed SWCNT-TFT is in a top-gated configuration. It consists of source (S) and drain (D) electrodes, a carrier transport layer based on the purified SWCNT thin film, a gate dielectric layer, and a top gate electrode (G). The highly pure, additive-free, aqueous, SWCNT ink is prepared by Brewer Science Inc. The average tube diameter of the SWCNT is 0.8 nm. The length of the SWCNT varies from a few hundred nm to 1 $\mu$m. The trace metal impurity concentration is measured to be <500 ppb. The width ($W$) of the source and drain electrodes is 500 $\mu$m, and the separation between the source and drain electrodes, that is, channel length ($L$), is 50 $\mu$m. All of these TFT elements were printed on a DuPont Kapton FPC polyimide film [15] by using an Optomec's Aerosol Jet printing system [16]. The source and drain electrodes were first printed on the Kapton FPC polyimide film using UTD Ag silver nanoink from UT-Dots. The active carrier transport layer was then printed, followed by the printing of the gate. Detailed printing process of the SWCNT-TFT is reported elsewhere [10].

## 3. Results and Discussion

Figure 1 shows the source-drain $I$-$V$ characteristics ($I_D$ versus $V_{DS}$) of the SWCNT-TFT at different gate voltages ($V_G$) from −2.0 V to +2.0 V. At the same source-drain voltage ($V_{DS}$), the drain current ($I_D$) decreases as the gate voltage increases from −2.0 V to 2.0 V, suggesting that the SWCNT layer is a p-type carrier (hole) transportation channel [10]. At low source-drain voltages $|V_{DS}| < 1.0$ V, the gate voltage of +2.0 V can effectively reduce the drain current.

At a gate bias of 0 V, a turn-on voltage of 1.0 V is observed, indicating Schottky barriers formed between the CNT and the source (S) and drain (D) electrodes. At the gate biases of 1.0 V and 2.0 V, a larger turn-on voltages of 1.3 V and 1.4 V are measured, respectively. This reflects that the SWCNT band-bending can be tuned by the gate bias, which changes the Schottky barriers and leads to the turn-on voltage variations. At a gate bias of −1.0 V, a nearly linear $I$-$V$ curve is obtained, indicating the transition from Schottky barrier to Ohmic contact at the SWCNT and the $S$ and $D$ electrode interfaces.

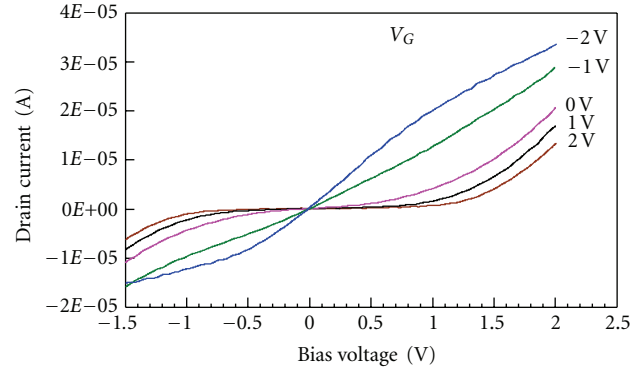


Figure 1: Source-drain $I$-$V$ characteristics ($I_D$ versus $V_{DS}$) of the CNT-TFT at different gate voltages ($V_G$). At the same source-drain voltage ($V_{DS}$), the drain current ($I_D$) decreases as the gate voltage increases from −2.0 V to 2.0 V, suggesting that the SWCNT layer is a p-type carrier (hole) transportation channel.

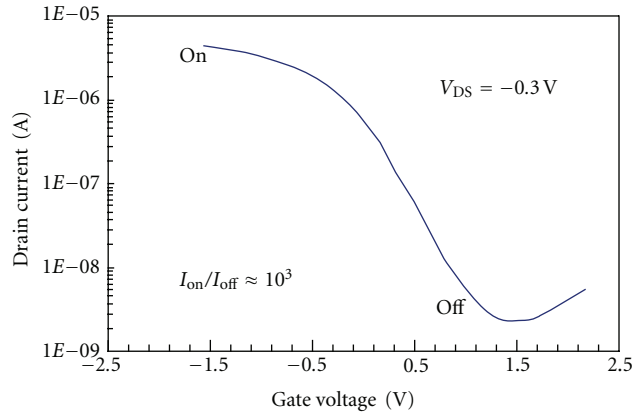


Figure 2: Drain current $I_D$ versus $V_G$ curves at the source-drain voltage $V_{DS}$ of −0.3 V. A high ON/OFF ratio of $\sim 10^3$ is obtained.

Figure 2 shows the drain current, the $I_D$, versus $V_G$ curve at the source-drain voltages $V_{DS}$ of −0.3 V. As the gate voltage $V_G$ increases from −2.0 V to +2.0 V, the drain current voltages $I_D$ decreases from $5.3 \times 10^{-6}$ (A) to $5.4 \times 10^{-9}$ (A). If one defines ON and OFF states to be the maximum and minimum steady drain currents $I_D$, respectively, a high ON/OFF ratio of $\sim 10^3$ is obtained with a low gate voltage tuning from −2.0 V to +2.0 V. Since metallic CNTs are conducting materials that are not affected by the gate field effect, the low drain current $I_D$ at the OFF state and the effective gate control of the SWCNT channel indicate that the concentration of the metallic CNT is low in the SWCNT-TFT and the SWCNT is primarily semiconducting CNT.

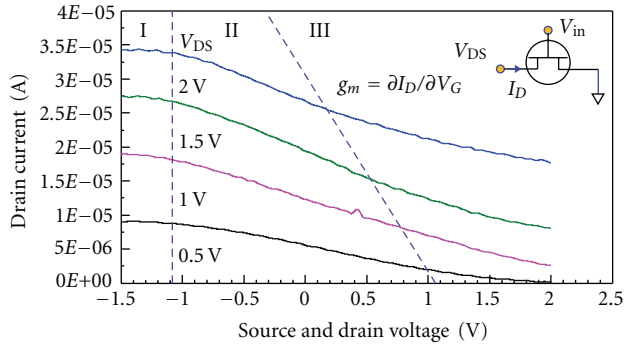


Figure 3: Drain current $I_D$ versus $V_G$ curves at different source-drain voltages $V_{DS}$. The inset shows the testing configuration. The $I_D$ versus $V_G$ curves can be divided into I, II, and III regions separated dashed lines.

Table 1: Transconductance at different $V_{DS}$ in the linear region.

| Source and drain voltage $V_{DS}$ | 0.5 V | 1.0 V | 1.5 V | 2.0 V |
|---|---|---|---|---|
| Transconductance $g_m$ | −3.5 $\mu$A/V | −5.7 $\mu$A/V | −7.4 $\mu$A/V | −7.5 $\mu$A/V |

Figure 3 shows the drain current $I_D$ versus $V_G$ curves at different source-drain voltages $V_{DS}$. The inset in Figure 3 shows the testing configuration. The $I_D$ versus $V_G$ curves can be divided into three regions separated by dashed lines. The three regions are marked in Figure 3 as I, II, and III, respectively. The regions have different transconductances $g_m = \partial I_D/\partial V_G$. Region I is when $V_G < -1.0$ V, the drain current $I_D$ varies little with the gate bias voltage $V_G$ (referred to as the saturation region henceforth). The transconductances in this region are low ($\sim -2\,\mu$A/V) for all the different source-drain voltages $V_{DS}$ from 0.5 V to 2.0 V. Region II is between the two dashed lines. In this region, the $I_D$ versus $V_G$ curves are linear (referred to the linear region henceforth). The transconductances $g_m$ at different $V_{DS}$ in the region are listed in Table 1.

In Table 1, it is shown that the transconductance varies little with $V_{DS}$ and it stays as a constant when $V_{DS} > 1.0$ V. For a conventional MOSFET, the drain current $I_D$ is related to the $V_{DS}$ in the linear region by the following equation [17]:

$$I_D = \frac{W}{L}\mu_n C_{ox}\left(V_G - V_T - \frac{V_{DS}}{2}\right)V_{DS}, \quad (1)$$

where $\mu_n$ is the mobility of an electron, $C_{ox}$ is the oxide capacitance per area, $L$ is the channel length, and $V_T$ is the threshold voltage. From (1), the transconductance of a conventional MOSFET $g_m = \partial I_D/\partial V_G$ is proportional to $V_{DS}$, whereas it is independent of $V_{DS}$ for the all-printed SWCNT-FET in Region II. The difference is attributed to the 1D quantum confined DOS of CNTs [12].

Region III is located to the right side of the second dashed line where the gate biases are positive. Figure 4 shows the logarithmic plots of the $I_D$ versus $V_G$ curves in this region. Linear dependence of natural logarithm of the drain current $\ln(I_D)$ on the gate voltage $V_G$ is obtained in this region,

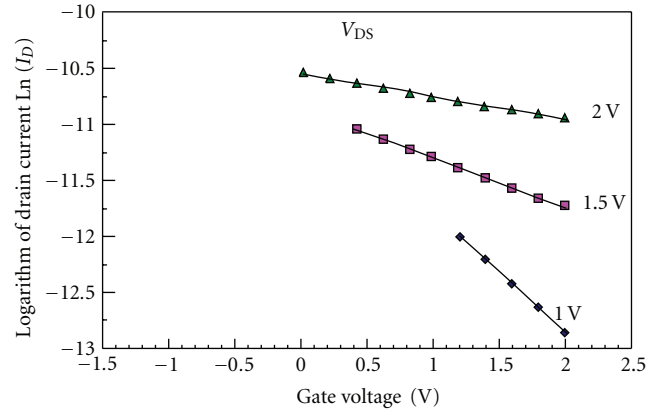


Figure 4: Logarithmic plots of the $I_D$ versus $V_G$ curves in the region III of Figure 3. The dashed lines indicated linear dependence of natural logarithm of the drain current $\ln(I_D)$ on the gate voltage $V_G$.

indicating exponential dependence of the drain current $I_D$ on the gate voltage $V_G$. This is similar to a conventional MOSFET in the subthreshold region [17]. The subthreshold slopes are calculated to be 2.1 V/decade, 5.2 V/decade, and 10.3 V/decade at the drain voltages of 1.0 V, 1.5 V, and 2.0 V, respectively. The subthreshold $I$-$V$ characteristics of an ideal CNT TFT can be expressed as [12]

$$I_D = \frac{4ekT}{h}\exp\left[\frac{e(V_G - V_T)}{kT}\right], \quad (2)$$

where $e$ is the charge of an electron, $h$ is the Planck's constant, $k$ is the Boltzmann's constant, and $V_T$ is the threshold voltage. Equation (2) shows that below threshold the drain current $I_D$ has an exponential dependence on $V_G - V_T$ at a rate of $kT/e = 26$ mV at room temperature $T = 300$ K. However, the printed SWCNT TFT shows a lower exponential dependence rate of 0.9 V, 2.2 V, and 4.5 V, at the drain voltages of 1.0 V, 1.5 V, and 2.0 V, respectively. The lower subthreshold slope was also reported [18]. This indicates that the gate bias has a less effective control of the drain current $I_D$ than the ideal CNT TFT. This is possibly due to the electric field screening of the gate bias due to the movement of local charges (electron or ions) stored in the gate dielectric [19]. This electric field screening effect is subject to further investigation.

## 4. Conclusion

In this paper, we demonstrated an all-printed flexible TFT based on the purified SWCNT solution. A high ON/OFF ratio of $\sim 10^3$ is obtained. The SWCNT-TFT also shows a linear transconductance region where the transconductance varies little with source and drain voltage bias $V_{DS}$. Subthreshold swings of the all printed TFT are also analyzed and agree well with the CVD-grown CNT-TFTs [12, 13]. The preliminary demonstration of the linear TFT with high ON/OFF ratio bias-independent transconductance indicates that all-printed flexible TFT based on the purified SWCNT solution is promising for analog RF electronics applications.

## Acknowledgments

This research is supported by AFOSR, under Award FA9550-08-1-0070, and NSF STTR Phase II, under Award IIP0924536, and NASA SBIR Phase II, under contract no. NNX09CA37C.

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